REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present case, Claims 22-27 were withdrawn from consideration as being directed to an unelected invention.

In the present Official Action, the drawings were first objected to under 37 C.F.R. 1.84(p)(5) as including a reference character ("41") having no definition in the specification. In response, the specification at page 24, corresponding to paragraph [0044] of the published application is being amended to recite element 41 as comprising a bit mapping 41 of the scan chain data. Respectfully, no new matter is being entered.

Furthermore, the drawings were objected to under 37 C.F.R. 1.83(a) as allegedly not showing every feature of the invention specified in the claims. Particularly, Claim 15 directed to the breakpoint being reached upon a predefined number of clock cycles must be shown.

In response, Applicants provide a Replacement Drawing Sheet showing propose to amend Fig. 3 to show a clock input to counter element 32 which is one embodiment for setting the breakpoint. Respectfully, no new matter is being entered as the amendment to Fig. 3 encapsulates the description provided at paragraphs [0034] and [0046], for example, that separate clocks (shown as element 37 in Fig. 3) are gated or halted upon reaching a predetermined count to allow operation of the logic macro to be stalled while running the EC fix within the FPGA.

Furthermore, the drawings were objected to under 37 C.F.R. 1.83(a) as allegedly not showing every feature of the invention specified in the claims. Particularly, Examiner indicates that Claim 28 setting forth "in-circuit emulator" and external "in-circuit emulator"

must be shown in the figures. In response, applicants delete the words in the subject matter of Claim 28, now incorporated in Claim 30.

Furthermore, the drawings were objected to under 37 C.F.R. 1.83(a) as allegedly not showing every feature of the invention specified in the claims. Particularly, Examiner indicates that Claim 30 setting forth "in the plurality of scan chains" must be shown in the figures or the feature canceled from the claim. In response, applicants respectfully submit that Fig. 2 illustrates "a plurality of scan chains data paths" for several logic functions with each of the logic functions associated with one (of a plurality) of embedded FPGAs operatively coupled thereto. It is understood that the scan latches (Fig. 3) associated with a logic function generates a scan chain data for that logic function that are fed to the one or more FPGA. However, to clarify the alleged deficiency in the drawings, Claim 30 is being amended to set forth the subject matter of Claim 2, namely, the provision of a plurality of scan chain data paths provided through the IC, and with one or more said embedded FPGAs being operatively connected for receiving a plurality of scan chains data from one more logic functions throughout the IC to correct data in the plurality of scan chain data paths through the IC (i.e., a scan chain defines a data path through the IC). Thus, the alleged phrase "the plurality of scan chains" has been modified in the claims to set forth plurality of scan chain data paths, as shown in Fig. 2. Respectfully, no new matter is being entered.

In view of the foregoing, the Examiner is respectfully requested to remove the drawing objections as indicated from paragraphs 2. –5. of the Office Action.

Further in the Office Action, Claim 28 was objected to due to a minor informality in line 17. It is noted that the subject matter of Claims 28-29 are being canceled and the subject matter thereof incorporated in Claim 30, now amended and re-cast in independent form. In

amended Claim 30, applicants have taken care to correct the informality in the manner as suggested by the Examiner. The Examiner is respectfully requested to remove the objection to Claim 28 (now Claim 30).

Further in the Office Action, Claim 2 was rejected under 35 U.S.C. §112, second paragraph, with the Examiner indicating as allegedly indefinite, the recitation of "implementing error correction" as being vague due to prior recitations containing the term "error correction". It is noted that the subject matter of Claims 1-2 are being canceled and the subject matter thereof incorporated in Claim 3, now amended and re-cast in independent form. In amended Claim 3, applicants have taken care to clarify the informality by modifying the defective phrase to now set forth: scanning data from the defective logic function into the FPGA and the registers and associated circuitry to implement error correction of the defective logic function. Respectfully, no new matter is being entered.

Further in the Office Action, Claim 5 was rejected under 35 U.S.C. §112, second paragraph, with the Examiner indicating as allegedly indefinite, the recitation of "the logic function IC" as having no antecedent basis. In response, applicants have amended Claim 5 in the manner to set forth: one or more logic functions within an IC. Respectfully, no new matter is being entered (See Fig. 2 of the present application). Claims 5 and 6 were further amended to obviate the further rejection of Claims 5 and 6 indicated by the Examiner in paragraph 10 of the office action. For example, the alleged phrase in claim 5 "strategically placed throughout the IC" alleged as not being a positive limitation, is now obviated by the new recitation in amended Claim 5 setting forth: ...the embedded FPGAs are operatively connected for receiving scan chain data from one or more logic functions within an IC. Claim

6 has been similarly amended. Respectfully, no new matter is being entered as full support is found in Fig. 2 of the present application.

Further in the Office Action, Claim 9 was rejected under 35 U.S.C. §112, second paragraph, with the Examiner indicating as allegedly indefinite, the recitation of language "such that...". In response, Applicants amend the Claim 9 to remove the entire phrase containing the offending recitation, and replaces the phrase with the following: "selecting and implementing a correction solution comprising one or more of: correcting bad data bits, correcting upstream data, or correcting downstream data. Respectfully, no new matter is being entered.

Further in the Office Action, Claim 10 was rejected under 35 U.S.C. §112, second paragraph, with the Examiner indicating as allegedly indefinite, the recitation of "defective logic function" as being vague. In response, applicants amend Claim 10 to set forth "a defective logic function of said identified defective logic functions". Respectfully, no new matter is being entered.

Further in the Office Action, Claim 19 was rejected under 35 U.S.C. §112, second paragraph, with the Examiner indicating as allegedly indefinite, the recitation of "the scan chain data" as having no antecedent basis. In response, applicants have amended Claim 19 in the manner to introduce a term "the scan chain data stream" which now provides proper antecedent basis for the later recited recited phrase: said scan chain data stream being captured in input latches. Claim 19 was further rejected as comprising an alleged indefinite phrase "...an incoming scan chain data stream..". In response, Claim 19 is being amended to set forth to remove the term "an incoming" and further setting forth said scan chain data

stream with antecedent basis being provided in the prior amendment to Claim 19, discussed above. Respectfully, no new matter is being entered.

Further in the Office Action, Claim 30 was rejected under 35 U.S.C. §112, second paragraph, as containing allegedly indefinite phrases, e.g., "the in-circuit emulator", "the logic function repair" and "the embedded FGPA being inserted into the scan chain..". Applicants have amended Claim 30 to obviate the indicated rejections either by removing the alleged vague recitation ("the in-circuit emulator") and re-characterizing the phraseology of the last paragraph in Claim 30 to wit:

> wherein a plurality of scan chain data paths are provided through the IC, and with one or more said embedded FPGAs being operatively connected for receiving respective scan chain data from one more logic functions throughout the IC to correct data in the plurality of scan data paths.

Respectfully, no new matter is being entered by the amendments to Claim 30.

In view of the foregoing, the Examiner is respectfully requested to withdraw all the rejections under 35 U.S.C. §112, second paragraph, of each of Claims 2 (now Claim 3), 5, 6, 9, 10, 19 and 30.

Further in the Office Action, the Examiner rejection Claims 1, 5, 28 and 29 under 35 U.S.C. §103(a), as being allegedly unpatentable over Bailis et al. (US 6,545,501). The Examiner however, did indicate that Claims 3-20, and Claim 30 presented allowable subject matter if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

In response, Applicants have amended claim 3 and cancelled claims 1 and 2 from further consideration in this application, and further, as mentioned above, has amended Claim

30 and have canceled Claim 28. Applicants are not conceding in this application that those canceled claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

It is noted that the dependencies of each of Claims 4-10, 13, 16-18 and 20 are being changed in view of the cancellation of Claim 1.

In view of the foregoing remarks herein, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned, Applicants' attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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